Post-Lab Report

ECEN 489 Lab 4 – Data Conversion Figures of Merit

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Introduction

This lab involves a series of simulations and experiments meant to test several data conversion figures of merit. The simulations cover everything from the SNR due to different types of noise and quantization, the SNR due to adjusting frequency with a lowpass filter, and the evaluation of an ADCs quality.

This is done by evaluating an ADC based on its characterization outputs to find the offset error, full scale error, transfer function, DNL, and INL. All of these can be used to evaluate the quality of an ADC.

Experimentally, a 3-bit flash ADC was created and its limits were tested similarly to the simulations. Its offset error, full-scale error, gain error, DNL, and INL were all calculated just as with the provided ADCs to evaluate.

Section 1: Modeling of a Zero-Order-Hold Sampling Circuit

Part 1: 200mV RMS Sinusoid applied to a 12-bit ADC with a 1.2V full-scale range

Note: The frequency was applied at 2MHz and the signal was sampled at 5MHz. This wasn’t mentioned in this lab but is consistent with the last two labs.

A:

A graph with a line

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Figure 1: Output FFT of a 200mV signal at 2MHz sampled at 5MHz with no noise and 12 bits

The averaged SNR for this waveform was calculated as -65.63689 dB. This was done with a very similar program to that of lab 2.

B:

A graph showing a normalized ftt of signal

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Figure 2: SNR of the input signal with Gaussian noise but without quantization

Before quantization, the SNR is quite bad at -10.472162 dB. This isn’t great, but the 2MHz signal can still be made out from the noise. This isn’t the case with the next simulation.

A graph of a normalized fft of signal

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Figure 3: SNR of the input signal with Gaussian noise and 12-bit quantization

With the Gaussian and quantization noise, the SNR of the output bits is absolutely terrible at -9.41607 dB. At this point with this sampling frequency, the signal can barely be made out.

C:

A graph showing a normalized fft of signal

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Figure 4: SNR of the input signal with uniform noise but without quantization

The SNR measured for this Fourier transform was -10.21799 dB. However, this ignores the DC signal. The noise magnitude is so large relative to the signal that it completely overwhelms it in some places. This causes a high DC value. The given SNR is ignoring any value at zero frequency. The same is done in the below scenario.

A graph showing a normalized fft of signal

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Figure 5: SNR of the input signal with uniform noise and with quantization

The SNR of the ADC output signal is measured at -9.590998 dB. This is slightly worse than the noise without quantization which is expected given that a slight amount of noise is added in.

Part 2: Calculation of an expression for the expression for the output SNR of an oversampled ADC + Lowpass filter

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Figure 6: Calculation of SNR as a function of “K” and number of quantization bits

The only change made here as opposed to the typical derivation of the SNR given the number of bits is that the lowpass filter will cut-out a factor of the quantization noise equal to the proportion of the sampling frequency that the signal bandwidth takes up.

As seen above, the ideal SNR given the oversampling factor “K” and the number of quantization bits can be given by:

Part 3: Derivation of factors for a 3-bit DAC with a 100mV LSB

A:

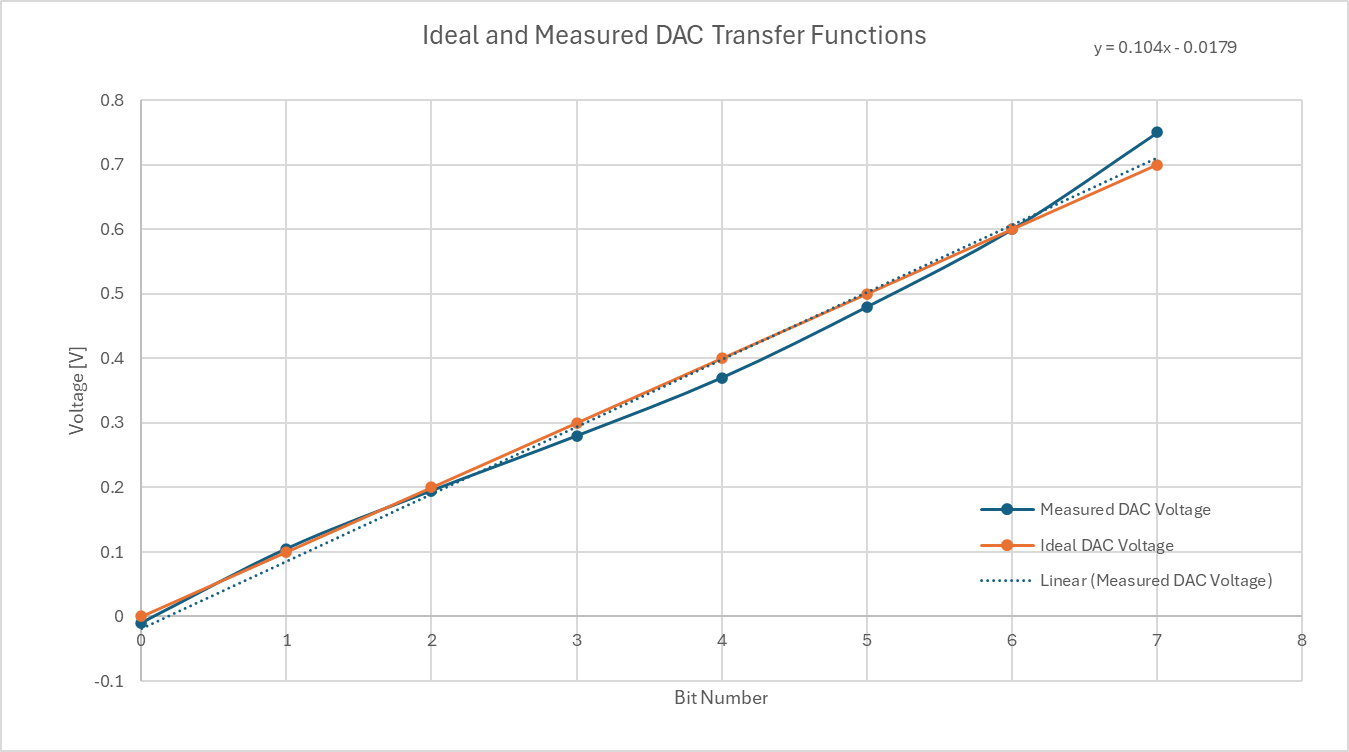


Figure 7: The graphed ideal and measured transfer function of the DAC along with its linear regression

From this, the offset can be determined by the y-intercept of the linear regression. The offset for this DAC is **-17.9mV**.

The full-scale error can be taken by combining the effects of the gain error and offset error by taking the full linear regression. In this instance, the regression line at the 7th bit results in a full-scale value of 710.1mV. This gives a full-scale error of **10.1mV** as the ideal value at the 7th bit is 700mV.

B:

For this question, the gain will be taken solely from the endpoint as that’s what is asked. The ideal gain taken by only the end point is [700mV/[100mV/LSB \* 7 LSB)] = 1 LSB/bit. The actual gain when calculated only by the endpoint of the measured can be found as [750mV/[100mV/LSB \* 7 LSB)] = 1.0714 LSB/bit. This gives a gain error of **0.0714 LSB/bit**.

C:

The end point corrected codes can be found in the table below. This was found by scaling the entire point set so that the highest point was equal to the ideal 700mV at the 7th bit. This was done by dividing each voltage measurement by a factor of approximately (760/700) and adding 0.0093. This is very similar to the gain error factor.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit Number | Original Voltage [V] | Endpoint Corrected Voltage [V] | DNL | INL |
| 0 | -0.01 | 0.000 |  |  |
| 1 | 0.105 | 0.106 | 0.0592 | 0.0592 |
| 2 | 0.195 | 0.189 | -0.1711 | -0.1118 |
| 3 | 0.28 | 0.267 | -0.2171 | -0.3289 |
| 4 | 0.37 | 0.350 | -0.1711 | -0.5000 |
| 5 | 0.48 | 0.451 | 0.0132 | -0.4868 |
| 6 | 0.6 | 0.562 | 0.1053 | -0.3816 |
| 7 | 0.75 | 0.700 | 0.3816 | 0.0000 |

Table 1: The original and endpoint-corrected voltages for the DAC along with the DNL and INL

Because the DNL is calculated as a relationship between two bits in an ADC, there is one row that is unfilled in the table above. This is to be expected. Additionally, the endpoint-corrected voltages for each bit and the DNL for each bit-pair is listed above.

The total INL listed above is the sum of each of the DNLs. Because these values are endpoint-corrected, it makes sense that the total INL is zero after the final DNL. The INL is taken as the sum DNL values up to and including the current bit that it is on.

D:

The maximum DNL can be taken directly from the table above and is clearly 0.3816 between the 6th and 7th bit

The maximum INL can also be taken from the table above and is clearly -0.500 after the 4th DNL.

Part 4: 4-bit ADC Characterization with ramp vector

Similarly to last time, the corrected voltages were taken by shifting the offset until the 0 binary combination is equal to 0V. Because the full-scale voltage isn’t known, the LSB is recalculated using the largest value as the output maximum. This allows the gain-error to be irrelevant.

To totally eliminate offset and full-scale errors, simply put the measured voltage through a linear regression. This is an easy and trivial way to take care of the errors.

The LSB for this was calculated as (202/15) = 13.4667

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit Number | Original Voltage | Endpoint Corrected Voltage | DNL | INL |
| 0 | 40 | 0 | -0.777 | -0.7772 |
| 1 | 43 | 3 | 0.262 | -0.5149 |
| 2 | 60 | 20 | 0.114 | -0.4010 |
| 3 | 75 | 35 | -0.257 | -0.6584 |
| 4 | 85 | 45 | -0.257 | -0.9158 |
| 5 | 95 | 55 | -1.000 | -1.9158 |
| 6 | 95 | 55 | -0.554 | -2.4703 |
| 7 | 101 | 61 | 0.040 | -2.4307 |
| 8 | 115 | 75 | -1.000 | -3.4307 |
| 9 | 115 | 75 | -0.629 | -4.0594 |
| 10 | 120 | 80 | -0.851 | -4.9109 |
| 11 | 122 | 82 | -0.777 | -5.6881 |
| 12 | 125 | 85 | 0.559 | -5.1287 |
| 13 | 146 | 106 | 0.782 | -4.3465 |
| 14 | 170 | 130 | 4.347 | 0.0000 |
| 15 | 242 | 202 |  |  |

Table 2: The sorted voltage, DNL, and cumulative INL of the given vector

Similarly to last time, the DNL was taken as the normalized difference between two adjacent bits from the ideal LSB difference and the INL is the sum of all DNLs up to that bit. Because of the endpoint correction, it again makes sense that the total cumulative INL is zero.

B:

From this, the peak DNL can be found to be 4.347 between the 14th and 15th bit.

The peak INL can also be clearly seen as -5.6881 after the 11th – 12th bit DNL is added.

C: This ADC is monotonic because of an assumption made in the processing of the data. It was assumed that the values were provided non-sequentially as sampled data. Because the given vector is interpreted as sampled data, not a list of values in order corresponding to the bit output, the data was sorted by magnitude before calculations were made. This resulted in the ADC being monotonic because of this assumption.

Part 5: 3-Bit ADC with provided DNL

A:

The INL of this ADC can be found very easily because the DNL is already provided. The INL is given to the right and is a cumulative sum of every DNL value up to that point

|  |  |  |
| --- | --- | --- |
| Bit Number | DNL | INL |
| 0 | 0 | 0 |
| 1 | -0.5 | -0.5 |
| 2 | 0 | -0.5 |
| 3 | 0.5 | 0 |
| 4 | -1 | -1 |
| 5 | 0.5 | -0.5 |
| 6 | 0.5 | 0 |
| 7 | 0 | 0 |

Table 3: The bit number and INL that correspond to the provided DNL

From this, the maximum INL can be seen as -1 LSB at the 4th bit. Additionally, it is expected that the final (or first) DNL is zero as there would be no values after (or before) it to compare it to.

B:

With the provided data, the offset error is equivalent to the full-scale error. Because of this, it can be assumed that there is no gain error in this function. Additionally, the DNL between the 0th and 1st bit is assumed to be zero and the final row of the DNL table is extra and shall be omitted. This is because, if the first row is assumed to be the DNL between bit 0 and 1, the final row will be the DNL between bits 7 and 8. As this is impossible, it will be omitted.

A graph with a line going up

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Figure 8: Plotted Transfer function of the provided 3-bit ADC

Part 6: Preamplifier/Latch Circuit Analysis

A diagram of a circuit

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Figure 9: Circuit that analysis will be performed on

A: General Explanation of the circuit

Phase 1 Inactive (0)

In this instance, transistors M1 and M2 are off as no current is allowed to flow through them. This isolates the input of the circuit from the output.

The transistors M3 and M4 are always on as the Vgs is permanently set to 1.5V. This makes it so that the only current difference can come from the inputs. Initially, one of the MOSFETs (M3 or M4) will be in triode (at virtually zero current) and the other will be in saturation depending on the previous state of the output latch. This is because, at the start of the phase, one of the nodes output will be at practically zero while the other will be at VDD.

Following that, the transistors M3 and M4 will both pull the two outputs towards VDD and eventually go into the triode region.

During this, M5 and M6 will both be pulled into saturation as their sources will be connected to ground and their gates will both approach VDD.

Phase 1 Active (1)

When phase 1 is active, the differential inputs of transistor M1 and M2 are “allowed” to influence the input to the latch and are in the amplification region. At the start of this stage, both output nodes are near VDD and the sources of transistors M5 and M6 are allowed to float. At this point, whichever input has the higher voltage (Vi+ for this example) will pull its respective output node lower faster.

In the case of Vi+ being larger, M1 will begin to overcome M3 faster than M2 will overcome M4. This means that the node at the gate of M6 will drop faster and turn “off” M6. This means that M5 will then conduct more current to whatever capacitance is at the sources of M5 and M6. This will push that node lower still thereby pushing the gate and source of M6 lower in tandem. This will decrease the current through M6 which will allow M4 to further pull the node to VDD, perpetuating the positive feedback by pushing M5 into triode mode – pulling its drain closer to its source.

In this specific scenario, M1 will approach the triode region as its drain drops and M2 will remain in saturation as its drain gets closer to VDD. M3 will be pushed into triode and M4 will remain in saturation for a similar reason. M5 will be pushed into triode while M6 will turn off as its gate further approaches its source.

B: Expression of the input vs the output

This expression will track the final voltage at the output as a function of the transistor transconductances and the capacitance at the output. It should be noted that this expression will stop and decrease as the node approaches VDD.

A diagram of a mathematical equation

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Figure 10: A model for the transitioning of the node labelled Vx until it reaches the threshold of the transistor M5 or M6

Once one of the Vx values reaches the threshold value of the transistors M5 or M6, that transistor will enter the triode region and begin to contribute to the positive feedback according to the model below:

A math equations on a white background

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Figure 11: A model for the transition of the node marked with Cn

This node will the be pulled towards zero along with its gate (Vx). This perpetuates the positive feedback cycle and the nodes will eventually saturate at 0V and VDD respectively. The equation in figure 10 for Vneutral will still hold true as the charge gained will eventually be pulled high because of the positive feedback.

C: Dynamic vs Static latches

Dynamic latches are latches that change their state and don’t remain the same throughout a cycle while static latches maintain relatively the same state despite the circuit’s changes. Dynamic latches include circuits like precharge evaluated latches while static latches include basic comparators.

Dynamic latches are much lower power than static latches as they have a set charge that they must dissipate each cycle. They involve a precharge and an evaluation stage where that charge is dissipated. Because of this, they can be incredibly fast as well. The downsides to this is that they can be volatile and leak their charge. If the charge is lost between the precharge and evaluation phase, the results can be entirely inaccurate. Because of this, they are also sensitive to longer time periods or anything that could alter the sensitive precharge nodes.

Static latches don’t require any charging or precharge phase. They are incredibly stable and maintain their information through positive feedback. This means that they are constantly refreshed and aren’t susceptible to charge dissipation like dynamic latches and are very good for long term charges. However, because of this feedback, they are much slower and require time to reach a definitive state. They also require more transistors for this feedback and the positive feedback circuits will consume quiescent current which means a higher active power consumption for storage.

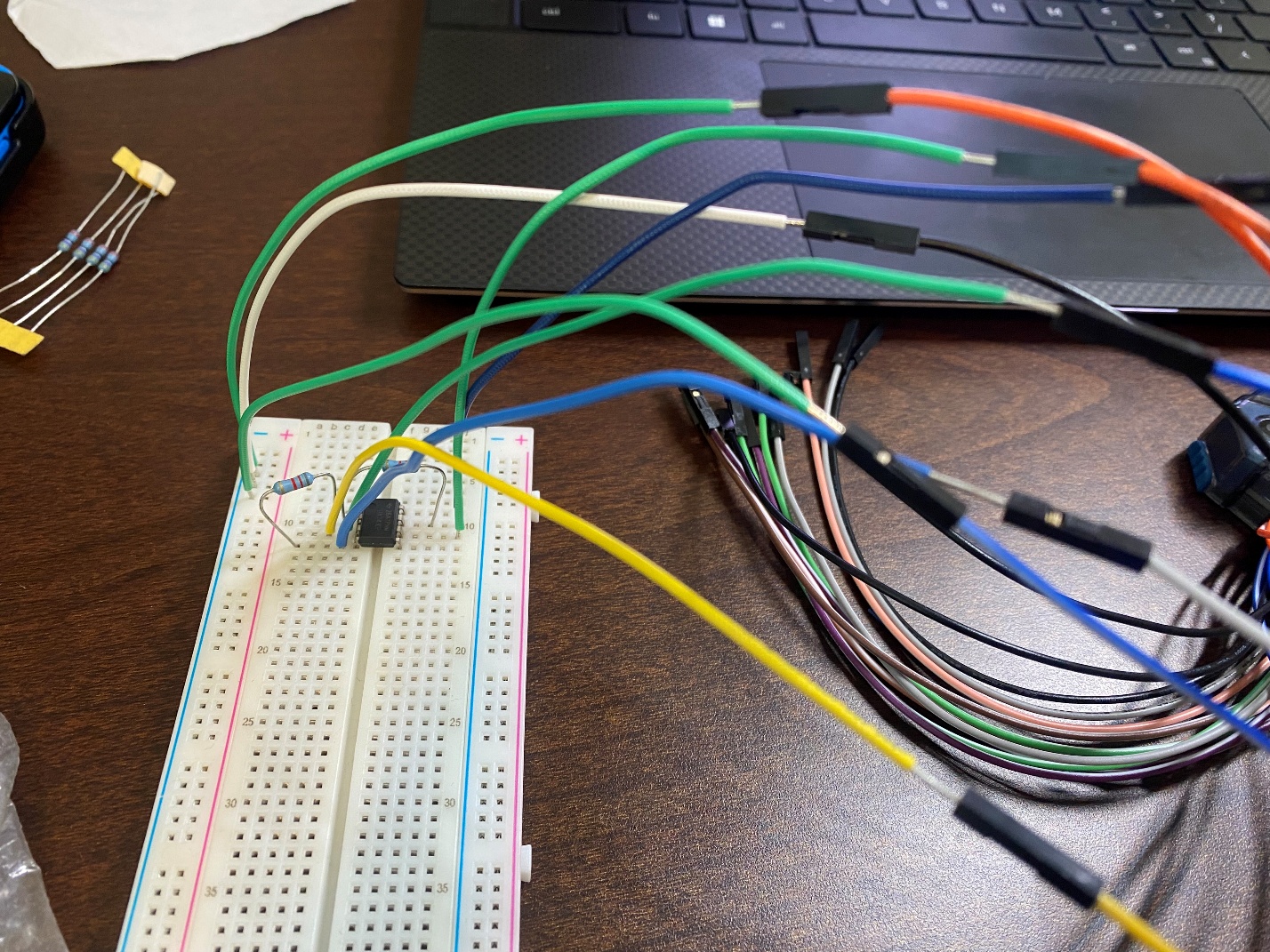
D:

This latch is a semi-dynamic latch. This is because it has a clocked cycle where information is imparted onto the latch. This clocked cycle involves a precharge phase which is then evaluated. This makes the latch dynamic. The static factor is in the feedback. Because it is a fed-back latch to ensure it locks into a state, it can be partially classified as static. However, because of the low capacitance and lack of charge-reinforcement, it is susceptible to charge leakage. This also makes it a dynamic latch.

Overall, the precharge/evaluate stage combined with the positive feedback and its susceptibility to charge-leakage make this a semi-dynamic latch.

Section 2: AD2 Based Work

Part 1: Single Comparator results



AD2 Figure 1: A picture of the circuit used to implement the single comparator

A screenshot of a computer

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AD2 Figure 2: The waveform of the comparator output when fed with a 1kHz sinewave

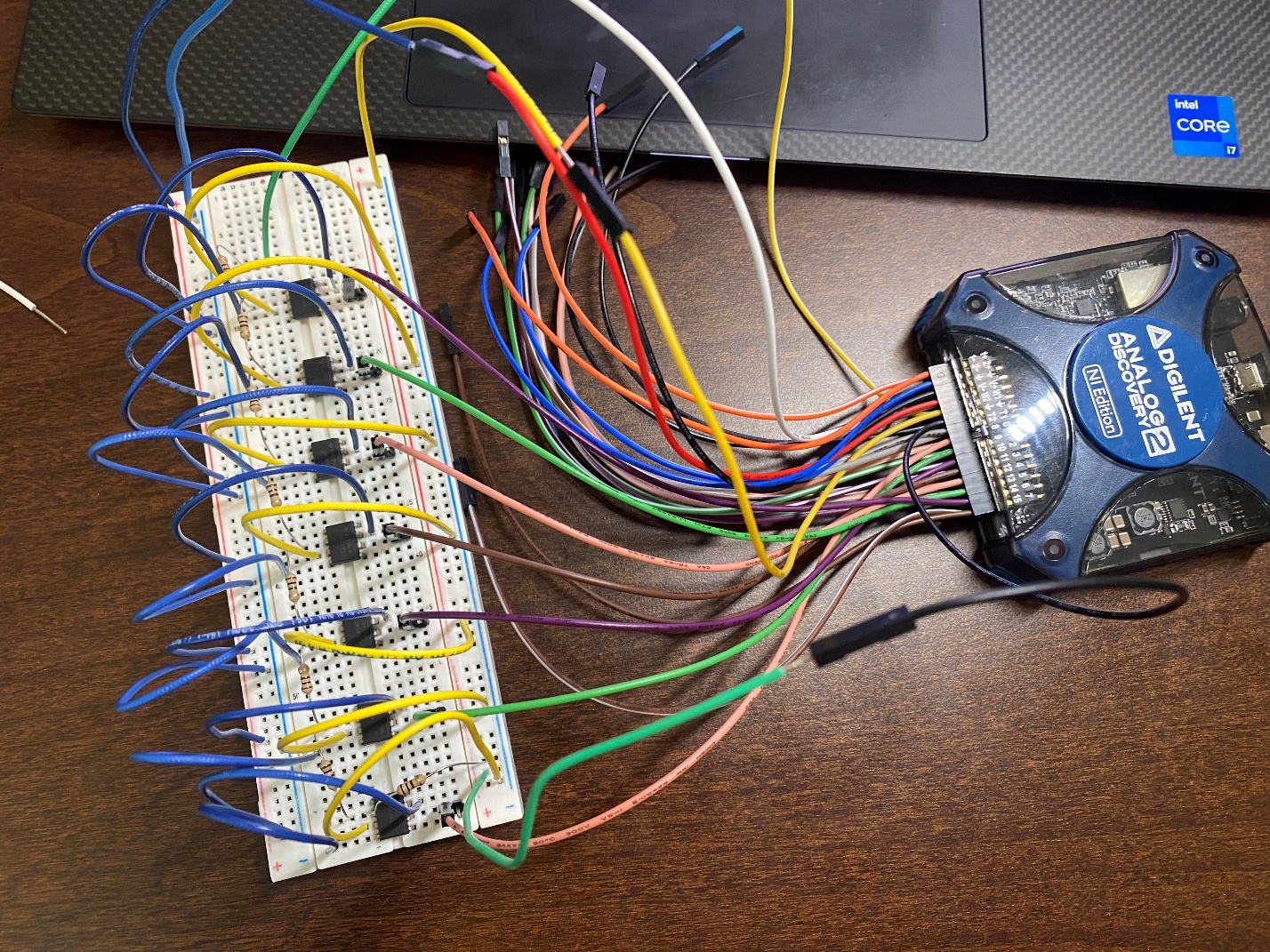
Note: the comparator is fed with +5V and -5V supplies and the reference voltage is set to approximately 0V. The input frequency was changed from 100kHz to 1kHz because the required output slew rate was too high for the 741 Op Amp.

Part 2: 3-Bit Flash ADC

In the construction of this 3-Bit ADC, some design choices were made. The comparators were designed to swing from 5V to -5V upon switching. This was done primarily to simplify the design and guarantee a digital value change was read. The two waveforms were used to generate the Vfs reference voltage and the input waveform. Additionally, the LSB was said that it must be 100mV. To do this with an 3-Bit flash ADC, the full-scale voltage was determined to be 800mV (2^3 \* LSB).

The reference waveform used in the first result figure was a 1kHz sinewave oscillation from 800mV to 0V and a ramp wave of the same magnitude in the second figure. In the transfer function for this, the digital values are recorded in 100mV segments, each represented by their center value (eg. 50mV, 150mV, …, 750mV).

This ADC could have been constructed to perfectly represent the ideal voltage range of 0 to (Vfs-Δ), however, this didn’t match up with the diagram we were given. Additionally, we were instructed to use resistors of the same value when creating the resistor divider.



ADC Figure 3: Picture of the physical implementation of the 3-bit flash ADC

A screenshot of a computer

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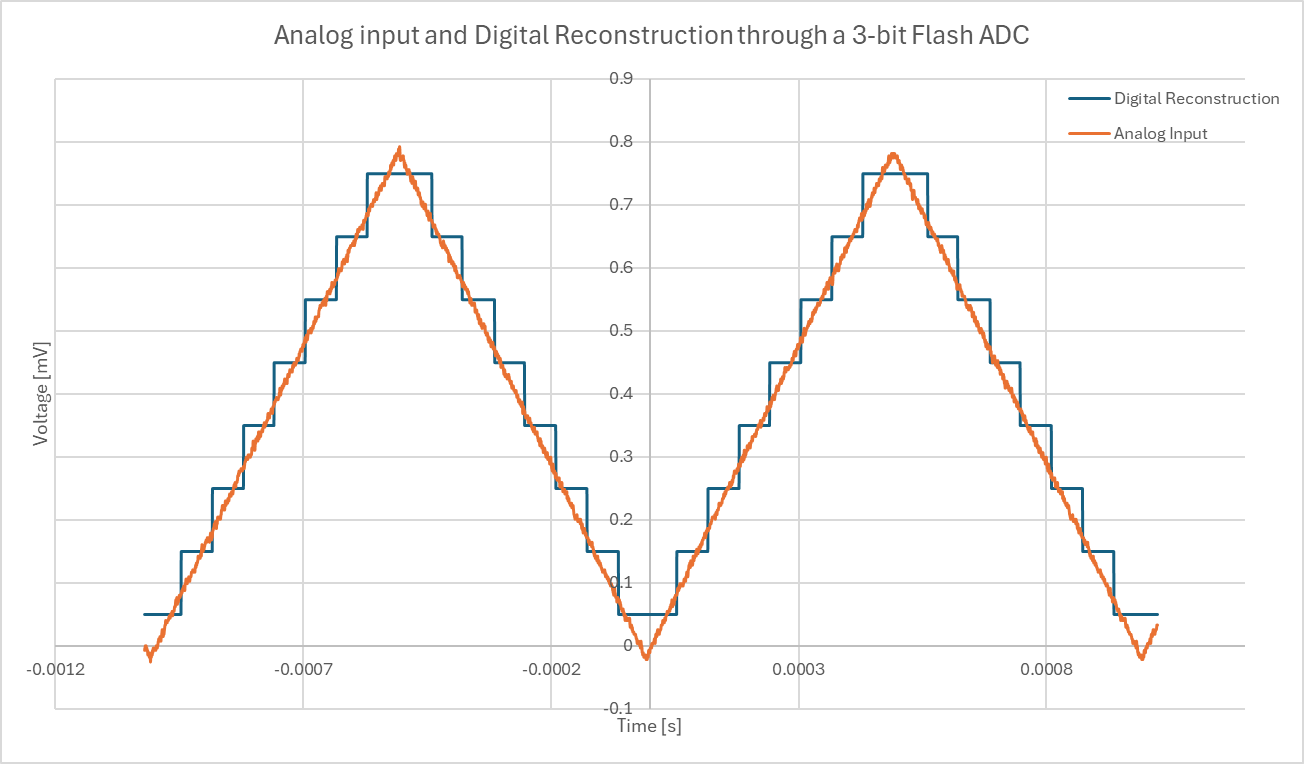
ADC Figure 4: Waveforms implementation of the ADC with 1kHz 0-800mV sinewave input

A screenshot of a computer

AI-generated content may be incorrect.

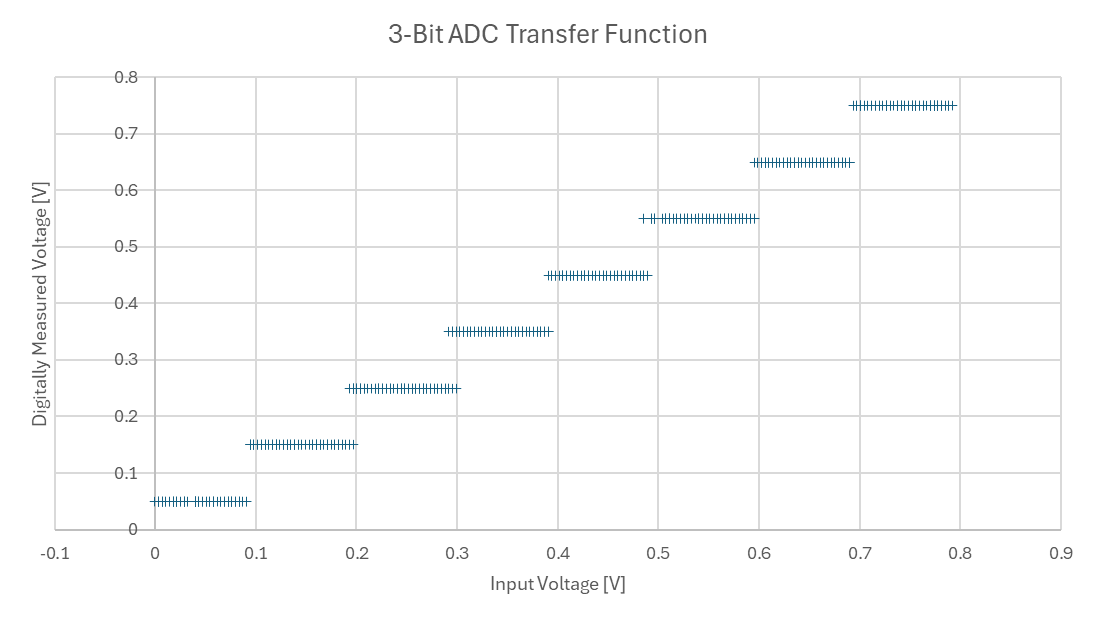
ADC Figure 5: Waveforms implementation of the ADC with 0-800mV ramp wave input

The digital data collected here was exported along with an oscilloscope measurement of the input waveform. The sum of the digital inputs at a given time was taken (to get the highest active bit) and then converted to the voltage input through a linear transformation.



ADC Figure 6: Time domain measurement of the digital reconstruction and analog input measurement

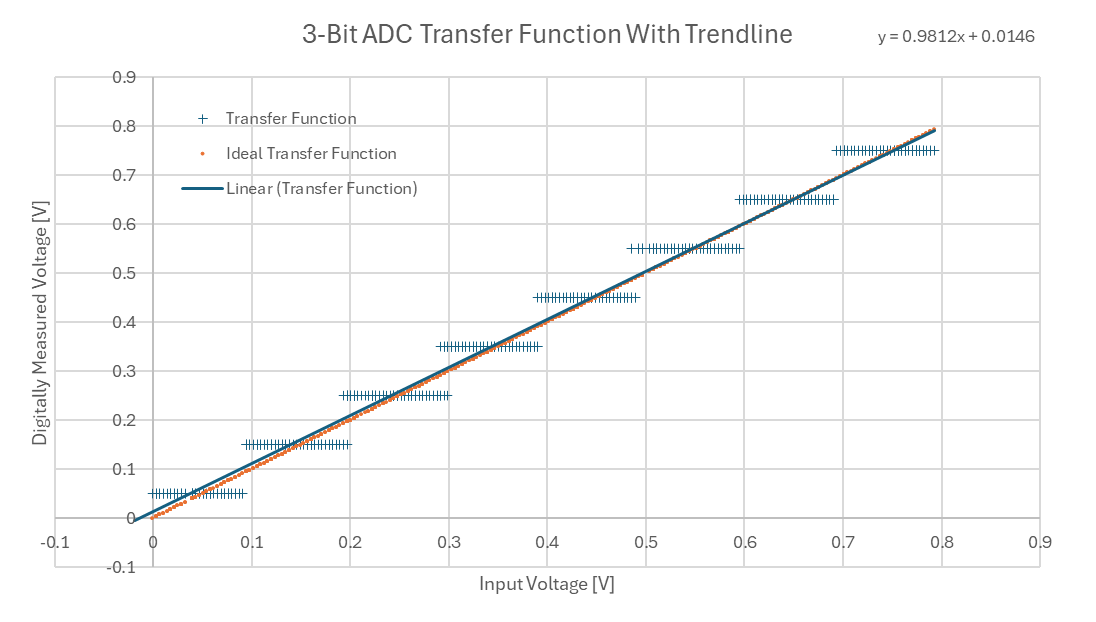
Part 4: Analysis and Transfer Function



ADC Figure 7: Transfer function derived from the time domain measurements above

It can be observed that, while this transfer function is very close to ideal, there are still some errors. One of these are that some measurements appear to transition very close to the required value while others are several millivolts off the mark.

To get the offset error of the ADC, a linear regression was performed on the measured data. The result was graphed and compared to the ideal transfer function below. The offset error was taken to be the y-intercept of the derived line as the ideal y-intercept would be 0V. The gain error can also be measured as the difference between the ideal gain and the trendline gain below.



ADC Figure 8: Measured offset error

Here, the offset error can be seen as **+14.6 mV**. The linear gain error can also be seen as approximately **1.88%** when referencing the ideal slope of the ADC. At 800mV, this gain error is approximately **15.04 mV**.

The full-scale error can be measured as the combined effects of the offset and gain error at the maximum voltage read by the ADC. In this case, these effects cancel each other out quite well. The difference between the ideal transfer function of the ADC and the measured transfer function of the ADC is approximately **440 uV.**

It’s a bit more difficult to measure differential and integral nonlinearity (DNL, INL). While this is a statistic that is primarily used in DACs, not ADCs, it can be used in an ADC as well. The range of voltages for a given bit level is subtracted from the ideal voltage range for that bit level then normalized to the ideal bit range (100mV). This is summarized in the table below.

|  |  |  |  |
| --- | --- | --- | --- |
| Bit Number | Voltage Range [mV] | Deviation [mV] | DNL |
| 1 | 91.35507228 | -8.64492772 | -0.08645 |
| 2 | 102.317681 | 2.317680953 | 0.023177 |
| 3 | 91.35507228 | -8.64492772 | -0.08645 |
| 4 | 95.00927517 | -4.99072483 | -0.04991 |
| 5 | 95.00927517 | -4.99072483 | -0.04991 |
| 6 | 109.6260867 | 9.626086735 | 0.096261 |
| 7 | 95.00927517 | -4.99072483 | -0.04991 |
| 8 | 116.9344925 | 16.93449252 | 0.169345 |
| Sum (INL) | | | -0.03384 |

ADC Table 1: Table detailing the DNL for each bit of the constructed ADC and the INL for the ADC overall

To summarize the voltage range is the difference between the greatest and smallest voltage values measured at each bit level. The deviation is how far off that was from the ideal value and the DNL was the deviation normalized to the value of the LSB (100mV). The INL is the sum of all the DNL values.

For each bit, the DNL ranges from 16.9% to -8.65%. These roughly cancel out to give an INL in the range of 3.38%.